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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 20020057446 A1	20020516	206	MULTI- INSTRUCTION STREAM PROCESSOR	358/1.13	358/1.15; 358/1.16;	
2	☐	☐	US 20010021971 A1	20010913	252	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR	712/215		
3	☐	☐	US 6414687 B1	20020702	201	Register setting-micro programming system	345/503	345/520; 345/559;	
4	☐	☐	US 6393549 B1	20020521	132	Instruction alignment unit for routing variable	712/204	712/215	
5	☐	☐	US 6393545 B1	20020521	201	Method apparatus and system for managing virtual memory	712/34	711/148; 711/153;	
6	☐	☐	US 6349379 B1	20020219	201	System for executing instructions having flag for	712/210	712/225	
7	☐	☐	US 6336180 B1	20020101	209	Method, apparatus and system for managing virtual memory	712/34	711/206; 711/207;	
8	☐	☐	US 6311258 B1	20011030	202	Data buffer apparatus and method for storing graphical	711/200	711/210; 711/211;	
9	☐	☐	US 6289138 B1	20010911	205	General image processor	382/307	382/308	
10	☐	☐	US 6272257 B1	20010807	301	Decoder of variable length codes	382/246		
11	☐	☐	US 6269436 B1	20010731	153	Superscalar microprocessor configured to predict return	712/23	712/228; 712/229;	

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
12	☐	☐	US 6260073 B1	20010710	76	Network switch including a switch manager for	709/249	370/412; 370/911;	
13	☐	☐	US 6259456 B1	20010710	295	Data normalization techniques	345/619	345/501	
14	☐	☐	US 6246396 B1	20010612	299	Cached color conversion method and apparatus	345/604	345/549; 345/600;	
15	☐	☐	US 6237079 B1	20010522	239	Coprocessor interface having pending instructions queue	712/34	711/153	
16	☐	☐	US 6195674 B1	20010227	311	Fast DCT apparatus	708/402	708/401	
17	☐	☐	US 6189068 B1	20010213	142	Superscalar microprocessor employing a data cache	711/3	711/118; 711/204;	
18	☐	☐	US 6131140 A	20001010	24	Integrated cache memory with system control logic and	711/104	711/100; 711/118;	
19	☐	☐	US 6118724 A	20000912	211	Memory controller architecture	365/230.05	365/189.02; 365/221;	
20	☐	☐	US 6079006 A	20000620	152	Stride-based data address prediction structure	711/213	711/221; 712/237;	
21	☐	☐	US 6061749 A	20000509	324	Transformation of a first dataword received from a	710/65	345/603; 345/643;	
22	☐	☐	US 6014734 A	20000111	150	Superscalar microprocessor configured to predict return	712/23	712/228; 712/229;	

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
23	☐	☐	US 6006324 A	19991221	136	High performance superscalar alignment unit	712/204	712/215	
24	☐	☐	US 5987561 A	19991116	146	Superscalar microprocessor employing a data cache	711/3	711/128; 711/204;	
25	☐	☐	US 5978907 A	19991102	145	Delayed update register for an array	712/239		
26	☐	☐	US 5968169 A	19991019	129	Superscalar microprocessor stack structure for judging	712/239		
27	☐	☐	US 5935239 A	19990810	144	Parallel mask decoder and method for generating said	712/224	712/213; 712/23;	
28	☐	☐	US 5933618 A	19990803	154	Speculative register storage for storing speculative	712/217	712/212; 712/213;	
29	☐	☐	US 5892936 A	19990406	140	Speculative register file for storing speculative	712/216	712/212; 712/213;	
30	☐	☐	US 5887152 A	19990323	130	Load/store unit with multiple oldest outstanding	712/217	711/136; 711/200;	
31	☐	☐	US 5881278 A	19990309	154	Return address prediction system which adjusts the	712/242	712/238	
32	☐	☐	US 5878255 A	19990302	137	Update unit for providing a delayed update to a branch	712/240		
33	☐	☐	US 5875324 A	19990223	147	Superscalar microprocessor which delays update of	712/238	712/240	

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
34	☐	☐	US 5875315 A	19990223	180	Parallel and scalable instruction scanning unit	712/204		
35	☐	☐	US 5867723 A	19990202	62	Advanced massively parallel computer with a secondary	712/11	711/114; 711/119;	
36	☐	☐	US 5864707 A	19990126	149	Superscalar microprocessor configured to predict return	712/23	712/228; 712/243	
37	☐	☐	US 5860104 A	19990112	149	Data cache which speculatively updates a	711/137	711/126; 711/204;	
38	☐	☐	US 5859991 A	19990112	155	Parallel and scalable method for identifying valid	712/204		
39	☐	☐	US 5854921 A	19981229	145	Stride-based data address prediction structure	712/239	712/1; 712/23	
40	☐	☐	US 5848433 A	19981208	133	Way prediction unit and a method for operating the	711/137	711/118; 711/125;	
41	☐	☐	US 5832297 A	19981103	136	Superscalar microprocessor load/store unit employing a	710/5	710/56; 710/6;	
42	☐	☐	US 5832249 A	19981103	134	High performance superscalar alignment unit	712/204	712/215	
43	☐	☐	US 5826071 A	19981020	146	Parallel mask decoder and method for generating said	712/224	712/23	
44	☐	☐	US 5822574 A	19981013	131	Functional unit with a pointer for mispredicted	712/233	712/215; 712/217;	

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Abstract Text - ABTX (1):

An integrated circuit and computer system.
According to one embodiment of the
present invention ar
single substrate for
microprocessor which
processor bus is pro
integrated circuit i
access memory array
logic control unit,
which is coupled to
access memory array
coupling to the processor bus. In
one embodiment, a further multiplexer having
an output for coupling to a first
portion of a memory is provided, and this
multiplexer further has input for
coupling to a second portion of the memory
bus. The IC according the present
invention is also for use with a second IC
which includes control logic for
controlling system memory and for
controlling the processor bus and memory bus

as well as interfacing to other buses such as
peripheral bus. The present
invention also provides for improved layout
of a cache array with a data path
logic management unit as well as power
management features for the cache array
and a tag RAM with comparator on, in one
embodiment, the same chip with the
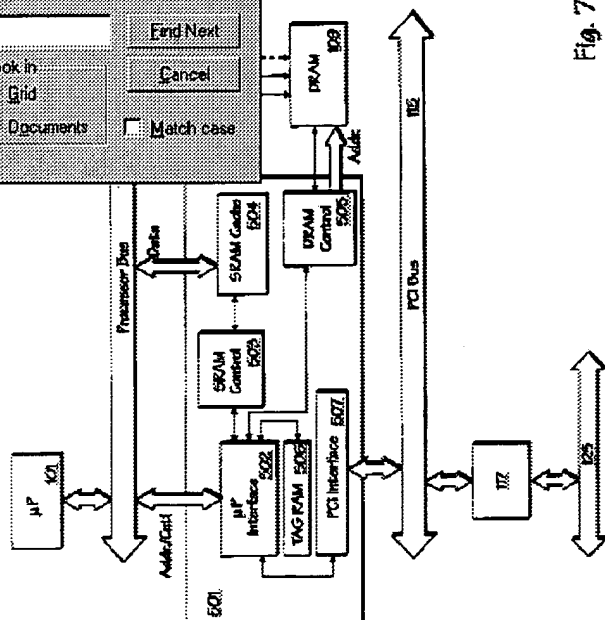cache array or on an associated chip in
another embodiment.

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Fig. 7

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L11: (17) 10 not 5 | US 6167491 A | Tag: S | Doc: 4/17 | Format : K...

L11: (17) 10 not 5 | US 6167491 | Tag: S | Doc: 4/17 | "Full" 1/32 (Total imag...

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output terminals 32 and 34. The write access
interface 26, under control of
the control interface 24, provides for
buffering, queuing and routing of data
for storage in the RAM core 28, the data
being communicated to the memory
circuit 22 at one or more of the data input
terminals 32. The read access
interface 30, under control of the control
interface 24, provides for routing,
queuing and buffering of data stored in the
RAM core 28 for communication at
one or more of the data output terminals 34.

Detailed Description Text - DETX (12):

The memory circuit 36 shown in FIG. 3 is a
specific embodiment of the memory
circuit 22 shown generally in FIG. 2. In
memory circuit 36, the control
interface 24 comprises a master control 40,
a load control 42, a RAM access
control 44, and an unload control 46. The
control interface 24, as shown, also
comprises a refresh control 48. The refresh
control 48 is employed when the

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United States Patent [19]

McAlpine

[11] Patent
[45] Date of

[54] HIGH PERFORMANCE DIGITAL
ELECTRONIC SYSTEM ARCHITECTURE
AND MEMORY CIRCUIT THEREFOR

[76] Inventor: Gary L. McAlpine, 11555 SW. 155th
Ter., Beaverton, Oreg. 97007

[21] Appl. No.: 09/035,640

[22] Filed: Mar. 5, 1998

Related U.S. Application Data

[62] Division of application No. 08/812,376, Mar. 5, 1997, Pat.
No. 5,802,580, which is a continuation of application No.
08/300,421, Sep. 1, 1994, abandoned.

[51] Int. Cl.⁷ G06F 12/02
[52] U.S. Cl. 711/149; 711/143; 711/146
[58] Field of Search 711/131, 149,
711/168, 143, 146

[56] References Cited

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Primary Examiner—Hiep T. Nguyen

[57]
A digital electronic s
system components
system components,
communicating data
digital electronic sy
control bus, coupled
nents and to the men
control signals amc
memory circuit is pr
of the ports (i) hav
terminal that transfer
operating independe
coupled respectively
for data communica
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placing in the queue
size of the block and
interface preferably c
selection circuit pref
selectable blocks of t
positions in selected
array is also provide
be written to the arr
the array a contiguou
block and its placeme
preferably comprises
circuit preferably is
able data received f
selectable positions

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Taylor

[45] **Date of Patent:** Dec. 1, 1998

[54] **DUAL PORT MEMORIES AND SYSTEMS AND METHODS USING THE SAME**

[75] Inventor: Ronald T. Taylor, Grapevine, Tex.

[73] Assignee: Cirrus Logic, Inc., Fremont, Calif.

[21] Appl. No.: 666,815

[22] Filed: Jun. 19, 1996

[51] Int. Cl.⁶ G11C 8/00
[52] U.S. Cl. 365/230.05; 365/230.03
[58] Field of Search 365/230.05, 230.03, 365/220

[56] **References Cited**

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Primary Examiner—David Nelms
Assistant Examiner—Hoai V. Ho
Attorney, Agent, or Firm—James J. Murphy; Steven A. Shaw

[57] **ABSTRACT**

A memory 20 includes a first array 100 and a second array 102 of memory cells. A first data port 118 allows for the exchange of data with the first array 100 and a second data port 120 allows for the exchange of data with the second array 102. Memory system 20 also includes a circuitry 122 for controlling data exchanges in a selected mode with the first array 100 via the first data port 118 and with the second array 102 via the second data port 120, the exchanges with the first and second arrays 100 and 102 being asynchronous.
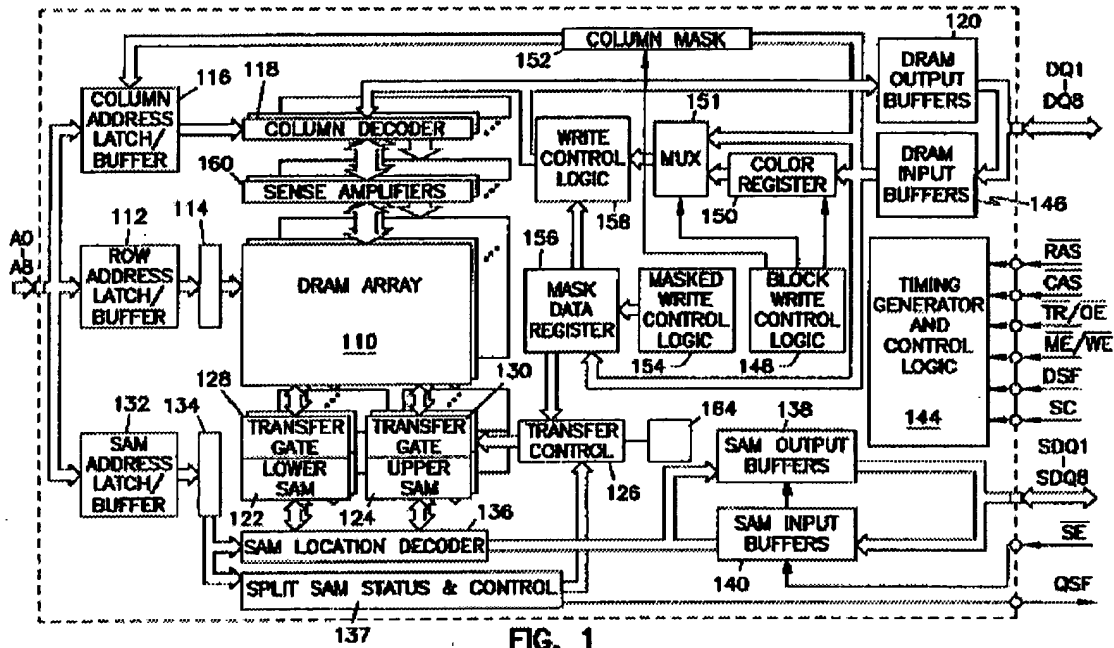
22 Claims, 4 Drawing Sheets

File Edit View Tools Window Help

U.S. Patent   Aug. 12, 1997   Sheet 1 of 13   5,657,266

COLUMN MASK 152

DRAM OUTPUT BUFFERS 120

DQ1 DQ8

COLUMN ADDRESS LATCH/ BUFFER 116 118

COLUMN DECODER 160

SENSE AMPLIFIERS

WRITE CONTROL LOGIC 158

151 MUX

COLOR REGISTER 150

DRAM INPUT BUFFERS 146

ROW ADDRESS LATCH/ BUFFER 112 114

A0 A8

DRAM ARRAY 110

MASK DATA REGISTER 156

MASKED WRITE CONTROL LOGIC 154

BLOCK WRITE CONTROL LOGIC 148

TIMING GENERATOR AND CONTROL LOGIC 144

RAS
CAS
TR/OE
ME/WE
DSF
SC

SAM ADDRESS LATCH/ BUFFER 132 134

TRANSFER GATE LOWER SAM 122

TRANSFER GATE UPPER SAM 124

128 130 136

TRANSFER CONTROL 126

184

SAM OUTPUT BUFFERS 138

SDQ1 SDQ8

SAM LOCATION DECODER

SPLIT SAM STATUS & CONTROL 137

SAM INPUT BUFFERS 140

SE

QSF

FIG. 1

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